AMENDMENTS TO THE CLAIMS:

Please amend claims 1, 2, 7 and 8 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(Currently Amended)* A semiconductor active backplane comprising a semiconductor substrate including an array of addressable active elements and first electrodes, wherein said addressable elements are electrically connected to respective first electrodes of said array such that said~~on a semiconductor substrate for selectively energising respective~~ first electrodes of the array can be selectively energised, wherein at least part of the region beneath at least one of said first electrodes is formed as a depletion region whereby in use it acts as a reverse biassed capacitative diode wherein at least one charge trapping implant is provided adjacent but spaced from said depletion region.

2. *(Currently Amended)* A semiconductor active backplane comprising a semiconductor substrate including an array of addressable active elements and first electrodes, wherein said addressable elements are electrically connected to respective first electrodes of said array such that said~~on a semiconductor substrate for selectively energising respective~~ first electrodes of the array can be selectively energised, wherein at least part of the region beneath at least one of said first electrodes is formed as a depletion region whereby in use it acts as a reverse biassed capacitative diode wherein a

guard ring is provided over or around the periphery of said depletion region to prevent or hinder charge carriers from crossing between the depletion region and the rest of the substrate.

3. *(Cancelled)*

4. *(Previously presented)* A semiconductor active backplane according to claim 1 wherein there is a single active element at each location of the array provided by a single transistor.

5. *(Previously presented)* A semiconductor active backplane according to claim 1 wherein the active element(s) have a MOS construction.

6. *(Previously presented)* A semiconductor active backplane according to claim 1 wherein substantially the whole of each active element is covered by a metallic conductor, or a pair of metallic conductors.

7. *(Currently Amended)* A semiconductor active backplane comprising a semiconductor substrate including an array of addressable active elements and first electrodes, wherein said addressable elements are electrically connected to respective first electrodes of said array such that said~~on a semiconductor substrate for energising respective~~ first electrodes of said array can be selectively energized, wherein the semiconductor substrate further comprises~~, and~~ first and second orthogonal sets of addressing conductors, a respective pair of addressing conductors, one from each set, being associated with the addressing of a corresponding active element, wherein

substantially the whole of each active element is covered by at least one of said addressing conductors in the form of a metallic conductor.

8. *(Currently Amended)* A semiconductor active backplane comprising a semiconductor substrate including an array of addressable active elements and first electrodes, wherein said addressable elements are electrically connected to respective first electrodes of said array such that said~~on a semiconductor substrate for energising respective~~ first electrodesof said array can be selectively energized, wherein the semiconductor substrate further comprises~~, and~~ first and second orthogonal sets of addressing conductors, a respective pair of addressing conductors, one from each set, being associated with the addressing of a corresponding active element, characterised in that substantially the whole of each element is covered by said pair of addressing conductors in the form of metallic conductors.

9. *(Previously presented)* A backplane according to claim 1 wherein the array of active elements is covered by an insulating layer, each said active element being connected to a metal electrode on said insulating layer, the array of said metal electrodes thus formed covering more than 65% of the area of said array.

10. *(Original)* A backplane according to any claim 9 wherein the said array of said metal electrodes covers more than 80% of the area of said array of addressable active elements.

11. *(Previously presented)* A backplane according to claim 2 wherein the array of active elements is covered by an insulating layer, each said active element being

connected to a metal electrode on said insulating layer, the array of said metal electrodes thus formed covering more than 65% of the area of said array.

12. *(Previously presented)* A backplane according to claim 7 wherein the array of active elements is covered by an insulating layer, each said active element being connected to a metal electrode on said insulating layer, the array of said metal electrodes thus formed covering more than 65% of the area of said array.

13. *(Previously presented)* A backplane according to claim 8 wherein the array of active elements is covered by an insulating layer, each said active element being connected to a metal electrode on said insulating layer, the array of said metal electrodes thus formed covering more than 65% of the area of said array.

14. *(Previously presented)* A semiconductor active backplane according to claim 2, wherein there is a single active element at each location of the array provided by a single transistor.

15. *(Previously presented)* A semiconductor active backplane according to claim 2, wherein the active elements are comprised of a MOS construction.

16. *(Previously presented)* A semiconductor active backplane according to claim 2, wherein substantially the whole of each active element is covered by at least one metallic conductor.